**CS 7260 - Internet Architecture & Protocols**

**Scribe – 8/27**

As discussed in the last class, In the case of priority encoder -

If Input = 0, the output is 0

If Input = 1, the output is 1

- **Programmable Priority Encoder**

In Programmable Priority Encoder (PPE) there is an additional input where user can specify a number K which becomes the starting point of our scan. There is an N-bit input I as before, together with an additional log N-bit input P. The PPE circuit must compute an output O such that O[j] = 1, where j is the first position beyond P (treated as a binary value) that has a nonzero bit in I.

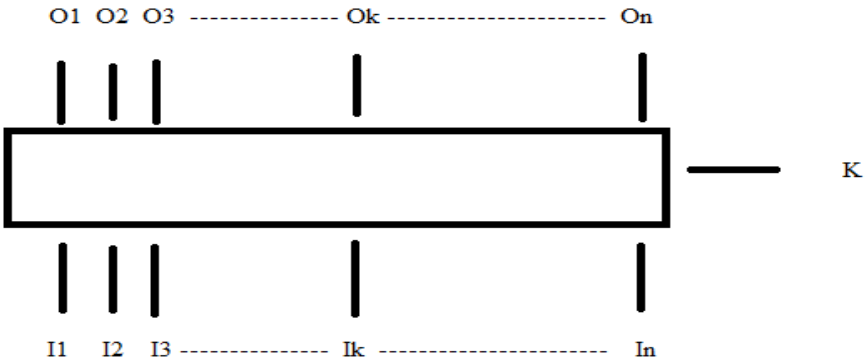


**Fig 1**: A Sample PPE. Here If Ik = 1, then Ok = 1

- A simple solution for PPE can be implemented as following

*"A barrel shifter can be used at the starting input bits to shift the bits to the left by (K-1) positions, after that we can feed the output of this barrel shifter to a simple Priority encoder. Then to get the desired output, we use another barrel shifter to shift the bits to the right by (K-1) positions."*

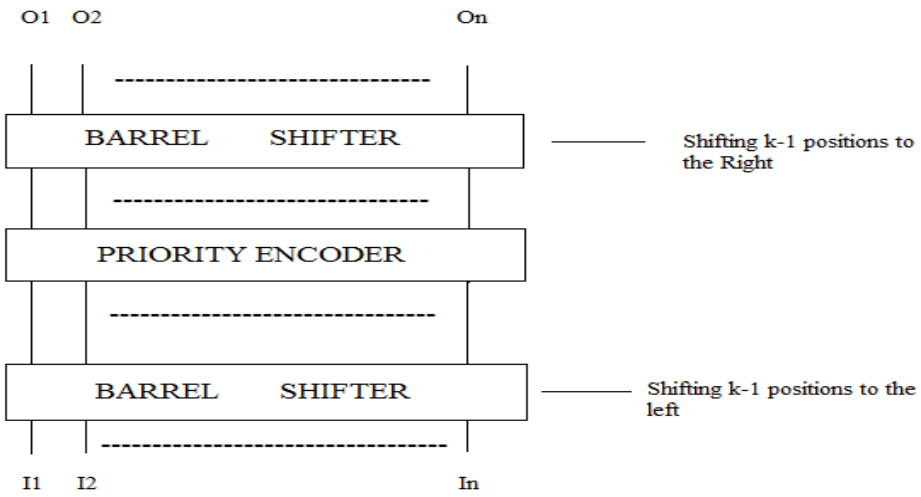


**Fig 2**: A Naïve Simple Solution for PPE

Now the question arises as to whether there should be a digital circuitry to subtract 1 from K? The answer would be a NO as this depends on the convention decided for the input Value (I). For e.g. , If we would have taken the first Input to be I0 instead of I1 , then there would have been no need of subtracting 1 from K.

**Calculating the Delay**: In the approach suggested above, a barrel shifter for N bits Input can be implemented using a tree of 2-input multiplexers in around log N time. Thus for the 2 barrel shifters and 1 Priority Encoder, the total gate delay becomes greater than equal to 3 Log N.

- Another way in which we can describe the PPE is that :

  "*If the input has some bit set at position K or higher than priority encode among bit positions k or higher else priority encode among the original Input*"

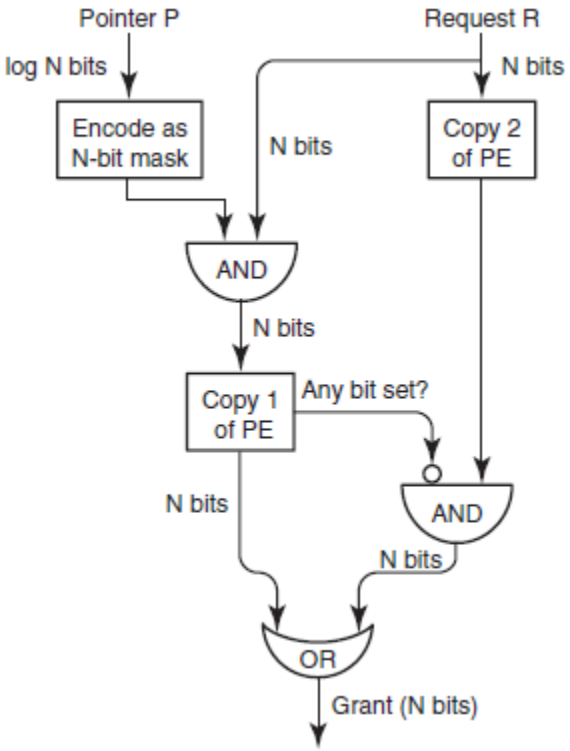


**Fig 3**: The design uses copy 1 of a priority encoder to find the highest bit set, if any, of all bits greater than P using a mask encoding of P. If such a bit is not found, the output of a second copy of a priority encoder is enabled using the bottom AND gate. The results of the two copies are then combined using an N-input OR gate.

**Calculating the Delay**: Here as we have split the problem into 2 ways, One where some bit is set after position P and the second where no bit is set. We are calculating the output accordingly as per the situation, so the overall delay gets reduced. Here, the gate delay will become 2Log N.

- **Memories**

Here we look at the different memory technologies which are available to us and the corresponding memory access time for each.

**Registers-** A register is an ordered collection of flip-flops

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|---|---|---|
| Access Delay | : | 0 – 5 nsec. |

**SRAM-** Stands for Static Random Access Memory. Contains N registers addressed by log N address bits.

| | | |
|---|---|---|
| Access Delay | : | 1-2 nsec (for on chip SRAM)<br>5-10 nsec (for off chip SRAM) |

**DRAM**- Stands for Dynamic Random Access Memory. Here, suppose we have to access a page of 512 bytes. In the case of DRAM to access the first byte, it will take around 40 or 50 nsec. After that for every other byte, it takes 1-2 nsec.

| | | |
|---|---|---|
| Access Delay | : | 40-60 nsec |

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References: Other than the lecture, I have referred the text book - Network Algorithmics by *George Varghese*